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Three-Dimensional Integrated Circuit With Embedded Microfluidic Cooling: Technology, Thermal Performance, and Electrical Implications

This paper reports on novel thermal testbeds with embedded micropin-fin heat sinks that were designed and microfabricated in silicon. Two micropin-fin arrays were presented, each with a nominal pin height of 200 μm and pin diameters of 90 μm and 30 μm. Single-phase and two-phase thermal testing of the micropin-fin array heat sinks were performed using de-ionized (DI) water as the coolant. The tested mass flow rate was 0.001 kg/s, and heat flux ranged from 30 W/cm^2 to 470 W/cm^2. The maximum heat transfer coefficient reached was 60 kW/m^2 K. The results obtained from the two testbeds were compared and analyzed, showing that density of the micropin-fins has a significant impact on thermal performance. The convective thermal resistance in the single-phase region was calculated and fitted to an empirical model. The model was then used to explore the tradeoff between the electrical and thermal performance in heat sink design.
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1 Introduction

Today, system performance and power dissipation are both constrained and are partly dictated by on- and off-chip interconnects [1,2]. Three-dimensional integrated circuits (3D ICs) with through silicon vias (TSVs) shorten the length of interconnects, which improves the performance and reduces the energy consumption of high-performance systems [3,4]. However, as increasing integration levels push the power density higher in 3D ICs, cooling becomes a major challenge [5–7]. The heat dissipation may exceed the capability of conventional air-cooled heat sinks. A switch from aircooling to microfluidic cooling is believed to be a promising solution [8]. Staggered cylindrical micropin-fin heat sinks are of particular interest because of their enhancement of surface area and high convective heat transfer [6]. Figure 1 shows one possible 3D IC scheme with an embedded micropin-fin heat sink. Stacked dice are cooled by liquid coolant flowing through the micropin-fins. The electrical interconnects are implemented by TSVs embedded in the micropin-fins.

The thermal performance of the heat sink is determined by the geometry of the heat sink, the coolant, the coolant flow rate, and its thermophysical properties. There has been significant prior research focused on this area. For signal-phase cooling, Tuckerman and Pease [9] demonstrated single-phase microfluidic cooling for the first time using DI water in 1981. By using microchannels (50 μm channel width, 50 μm wall width, and 302 μm cavity height), they were able to dissipate a heat flux of 790 W/cm^2 with maximum substrate temperature rise of 71 °C. Brunschwiler et al. [10] studied a three-tier single-phase

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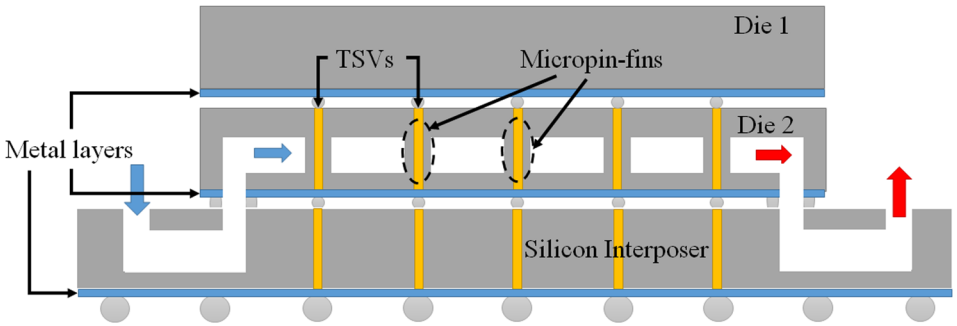

Fig. 1 Schematic of 3D IC with microfluidic cooling

microfluidic cooled 3D IC stack with a footprint of 1 cm^2 and maximum power of 390 W. They found that when the microchannel wall width equals the micropin-fin diameter (50 μm), with the same pitch (100 μm) and cavity height (100 μm), micropin-fin design has smaller convective thermal resistance in general while microchannels can improve cooling for strongly localized hotspots due to better tier-to-tier coupling. Peles et al. [11] investigated heat transfer and pressure drop phenomena of micropin-fin heat sinks for single-phase cooling. They concluded that cylindrical micropin-fin arrays are superior to plain microchannel based cooling.

For the two-phase cooling, Qu and Siu-Ho [12] studied flow boiling heat transfer of water in an array of staggered square micropin-fins covering an area of 3.38 cm length by 1 cm width. The cross section area of a single pin was 200 μm by 200 μm, and height was 670 μm. They observed that the two-phase heat transfer coefficient decreased with increasing heat flux at low quality and was fairly constant at a quality greater than 0.15. Reeser et al. [13] recently compared heat transfer and pressure drop characteristics of HFE-7200 and DI water in inline and staggered micropin-fin arrays. Studied heat fluxes ranged from 1 to 36 W/cm^2 and 10–110 W/cm^2 for HFE-7200 and water, respectively. Heat transfer coefficients behavior differed significantly for HFE-7200 and DI water due to different material properties of both working fluids. Kosar and Peles [14] studied flow boiling of R-123 for microhydrofoil shaped pin-fins. The heat transfer coefficient was found to increase with heat flux until a maximum was reached and then decreased monotonically with heat flux until critical heat flux was reached. Krishnamurthy and Peles [15] studied flow boiling of water in a 1.8 mm wide, 1 cm long, and 250 μm deep microchannel with staggered circular pin-fins. They found that the two-phase heat transfer coefficient was moderately dependent on mass flux, and independent of heat flux, for the range of mass fluxes and heat fluxes tested.

However, flow boiling of water in micropin-fin arrays at reduced pressures was rarely reported. By operating at reduced pressures, boiling in water can be initiated below 100 °C, which is desired for Si complementary metal-oxide semiconductor (CMOS). In this paper, two micropin-fin array heat sinks with different micropin-fin densities were fabricated and tested with heat sink outlet pressure below atmospheric pressure. Heat transfer performance of single-phase and two-phase flow in the micropin-fin area of both heat sinks was characterized and compared.

The heat sink design also impacts the electrical performance because the TSV dimensions and capacitance are affected by the geometry of the heat sink [6]. However, it is unknown how this will impact the electric signal performance at a circuit level. By introducing a compact circuit model, this paper analyzes the impact of microfluidic cooling on the signal path of a 3D interconnect link and the potential tradeoff between the thermal and electrical performance.

The paper is organized as follows: Section 2 introduces the design and fabrication process of the heat sinks; Section 3 summarizes the thermal testing results and analysis; the potential tradeoff between the thermal and electrical performance in 3D IC with embedded microfluidic cooling is shown in Sec. 4; and finally conclusions are drawn in Sec. 5.

2 Design and Fabrication

The heat sink testbed consists of a 1 cm × 1 cm array of staggered micropin-fins, as shown in Fig. 2. In addition to fluid inlet and outlet ports, pressure ports are included on both sides of the micropin-fin array in order to accurately measure pressure drop across the micropin-fin array while excluding pressure drop due to rapid flow constriction/expansion at the inlet and outlet ports. A single line of micropin-fins is also introduced on both sides of the micropin-fin array under test in order to promote an even flow distribution. Oval-shaped structures were added near the inlet and outlet for mechanical support. Four serpentine platinum heaters/resistance-temperature detectors generate heat load and provide temperature measurements in four sections along the flow length (between inlet and outlet). A fabricated sample can be seen in Fig. 2.

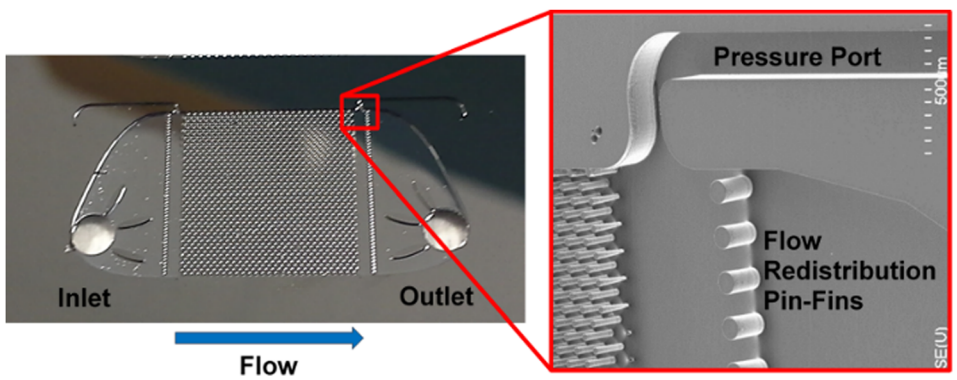

Fig. 2 Optical and scanning electron microscopy image of the heat sink

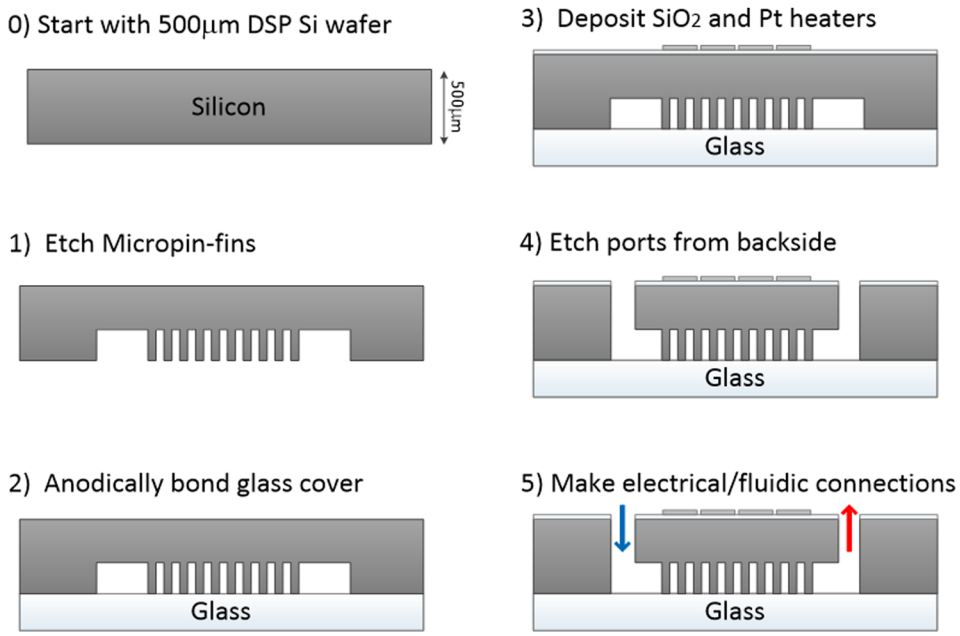

Fig. 3 Fabrication process of the heat sink sample

The process used to fabricate the heat sink testbed is shown in Fig. 3. The process begins with a 500 μm thick double-side polished wafer. A standard Bosch process with alternating SF_6 (for etching) and C_4F_8 (for passivation) was used to create the 200 μm ($\pm$5 μm) height micropin-fins and manifolds. The pitches and diameters of the micropin-fins can be different from die-to-die across the wafer. Next, the etched silicon wafer was cleaned with piranha solution (5:1 mixture of 98% sulfuric acid and 30% hydrogen peroxide) at 125 °C. The cavities formed during etching were then sealed using a Pyrex cap with anodic bonding with voltage of 800 V at 350 °C. The bonded wafer was then flipped and a 2 μm thick insulating silicon dioxide layer was deposited using chemical vapor deposition. Platinum heaters of 200 nm ($\pm$5 nm) thickness and 500 nm ($\pm$10 nm) thick gold pads were then deposited on the SiO_2 layer. Finally, inlet, outlet, and pressure measurement ports were etched using Bosch process from the same side of the wafer.

3 Thermal Testing

3.1 Test Setup and Procedure. The test flow loop consists of a gear pump, filter, flow meter, preheater, test section, heat exchanger, and fluid reservoir. The filter has a pore size of 7 μm and is used to remove contamination that may be present inside the flow loop system. The flow meter is used to measure the volumetric flow rate of the fluid, and it has a range of 50–500 mL/min. Heated fluid is condensed in the heat exchanger, which is cooled by a thermostatic bath circulator. The stainless steel fluid reservoir can hold up to 300 mL of fluid. Fluid pressure is measured at four locations, while temperature is measured at five locations. The measurement locations within the experimental facility are marked in Fig. 4.

The micropin-fin dimensions and arrangement are shown in Fig. 5. The transverse pitch, longitudinal pitch, and diameter are 135 μm, 225 μm, and 90 μm for sample 1 and 90 μm, 30 μm and

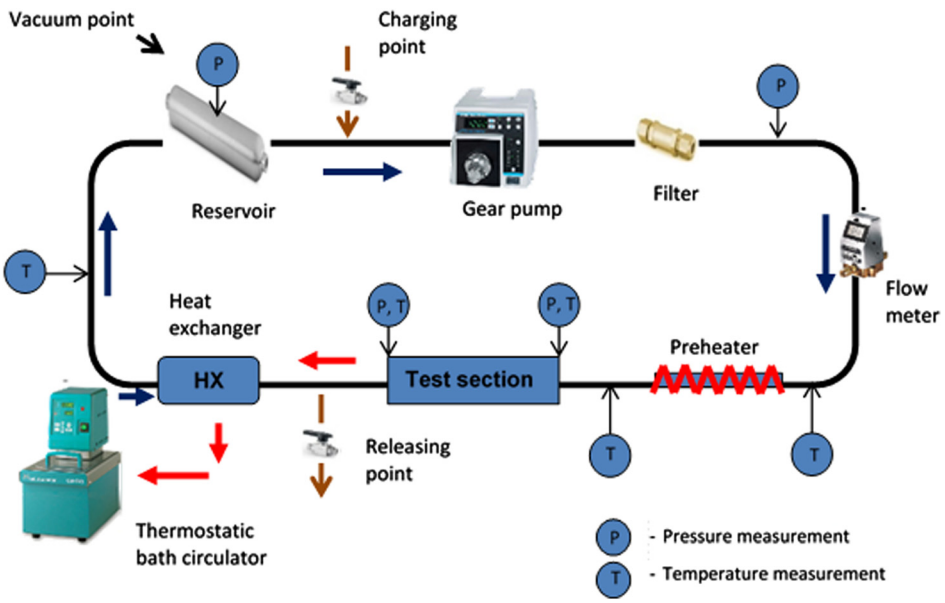

Fig. 4 Flow loop schematic

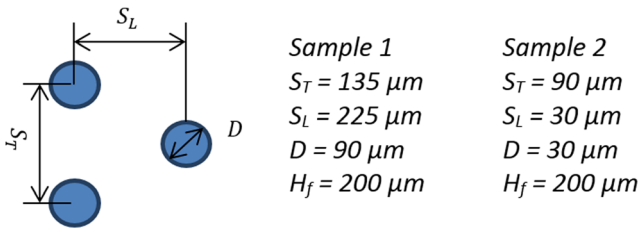

Fig. 5 Pin-fin array dimensions

Table 1 Testing parameters

	Sample 1	Sample 2
Mass flow rate (g/s)	1.07–1.09	0.97–1.06
Inlet temperature (°C)	5–8	12–18

Table 2 Uncertainty during testing

Flow rate	±0.8 mL/min
Pressure drop	±3 kPa
Fluid temperature	±0.5 °C
Wall temperature	±1.4 °C
Hear transfer coefficients	±0.5 kW/m^2 K
Heat flux	±0.1 W/cm^2

30 μm for sample 2, respectively. The micropin-fin height is 200 μm for both samples. Before testing, the heaters were calibrated in an oven to obtain the resistance-temperature curve for each heater from 20 to 145 °C. Heater resistance varies with temperature linearly. The calibrated device was packaged and then connected to the closed flow loop. The system was evacuated and charged with DI water. The DI water was boiled for 30 mins to remove any dissolved gas before charging the flow system. The testing parameters are summarized in Table 1, and the measurement uncertainty is shown in Table 2.

The mass flow rates for both samples were selected to be similar for fair comparison. The inlet temperature fluctuated because heat exchanger temperature on the cooling side fluctuated due to the limited ability of the thermostatic bath circulator to steadily control coolant temperature. Hydraulic and thermal characteristics were studied for single-phase and subcooled flow boiling of water.

3.2 Data Reduction and Results. Both single-phase and two-phase experiments were performed. To estimate heat loss, the power required to increase the water temperature from the inlet to the outlet was calculated and subtracted from the total power supplied to the heaters for single-phase experiments, as shown in the following equation:

$$Q_{\text{loss}} = P_{\text{total}} - \dot{m}C_{\text{p}}(T_{\text{out}} - T_{\text{in}}) \tag{1}$$

where $\dot{m}$ is the mass flow rate of water. The total power was calculated from the measured voltage and current of the heaters. The estimated heat loss percentage was about 11% for both devices at the highest heat flux for single-phase measurements, and this was applied to two-phase data to obtain effective heat flux.

Mass flux, G, is defined as

$$G = \frac{\dot{m}}{A_{c,\min}} \tag{2}$$

where $A_{c,\min}$ is the minimum cross-sectional area of the heat sink cavity. Thus,

$$A_{c,\min} = \left(W_{\text{ch}} - \frac{W_{\text{ch}}}{S_T}D\right)H_f \tag{3}$$

where W_{ch} and H_f are the heat sink cavity width and micropin-fin height, respectively. The effective heat flux is calculated as

$$q''_{\text{eff}} = \frac{P_{\text{total}} - Q_{\text{loss}}}{A_h} \tag{4}$$

where A_h is the total heated area.

The effective heat flux for single-phase can also be calculated as

$$q''_{\text{eff}} = \dot{m}C_{\text{p}}(T_{\text{out}} - T_{\text{in}}) \tag{5}$$

The single-phase heat transfer coefficient is calculated from the following equation:

$$q''_{\text{eff}}A_h = h_{\text{sp}}(\bar{T}_{m,w} - \bar{T}_{m,f})(\eta_f A_f N_t + A_h - N_t A_c) \tag{6}$$

where $\bar{T}_{m,w}$ and $\bar{T}_{m,f}$ are the mean wall temperature and the mean fluid temperature, respectively; A_f is the surface area of a single micropin-fin; A_C is the cross-sectional area of a single micropin-fin; and N_t is the total number of micropin-fins. Assuming that the micropin-fin tips are insulated, the fin efficiency η_f can be calculated using

$$\eta_f = \frac{\tanh(mH_f)}{mH_f} \tag{7}$$

where

$$m = \sqrt{\frac{h_{sp}P_f}{k_s A_c}} \tag{8}$$

where k_s is the solid material thermal conductivity, and P_f is the micropin-fin perimeter. The convective thermal resistance of a microfluidic heat sink gives a good metric for its heat removal capability; the convective resistance for single-phase is calculated using the overall fin efficiency η_o

$$R_{\text{CONV}} = \frac{1}{\eta_o h_{\text{sp}} A_t} \tag{9}$$

where A_t is the total area exposed to fluid, and $\eta_o = 1 - (NA_f/A_t)(1 - \eta_f)$.

The local two-phase heat transfer coefficient h_{tp} in a unit cell area containing a single micropin-fin is evaluated from

$$q''_{\text{eff}}A_{\text{uc}} = h_{\text{tp}}(A_{\text{uc}} - A_c)(T_w - T_{\text{sat}}) + h_{\text{tp}}\eta_f A_f (T_w - T_{\text{sat}}) \tag{10}$$

where A_{uc} is the base area of a unit cell. Thus,

$$A_{\text{uc}} = S_T S_L \tag{11}$$

where T_w is the micropin-fin base temperature over the last quarter of the chip, calculated from the last heater temperature, T_h. This is the region in which both liquid and gas phases exist. Assuming one-dimensional conduction in the heat sink base, T_w can be determined from

$$q''_{\text{eff}} = \frac{T_h - T_w}{\frac{t_{\text{Si}}}{k_{\text{Si}}} + \frac{t_{\text{SiO}_2}}{k_{\text{SiO}_2}}} \tag{12}$$

where t_{Si} and t_{SiO_2} are the thickness of silicon and silicon dioxide, and k_{Si} and k_{SiO_2} are the thermal conductivity of silicon and silicon dioxide.

The exit quality was calculated from

$$x = \left[\frac{q''_{\text{eff}}A_h - \dot{m}C_p(T_{\text{sat}} - T_{\text{in}})}{h_{\text{fg}}}\right] \Big/ \dot{m} \tag{13}$$

where T_{sat} and h_{fg} are the water saturation temperature and latent heat of vaporization, both of which are evaluated at device exit pressure.

Reynolds number is defined by

$$\text{Re} = \frac{\rho V_{\max} D}{\mu} \tag{14}$$

where ρ is the density, and μ is the dynamic viscosity. The maximum velocity of the fluidic $V_{\max}$ is defined by

$$V_{\max} = \frac{\dot{m}}{\rho A_{c,\min}} \tag{15}$$

The heat transfer coefficient, mean temperature difference from wall to fluid, convective thermal resistance, and pressure drop for both samples in the single-phase region are shown in Fig. 6. The single-phase heat transfer coefficient is almost independent of heat flux, as shown in Fig. 6(*a*). Sample 2, with higher pin density, has a lower heat transfer coefficient and higher pressure drop than sample 1, but at the same mean temperature difference from heat sink wall to fluid, sample 2 dissipates higher power than sample 1, as shown in Fig. 6(*b*). Sample 2 also has lower convective resistance as compared in Fig. 6(*c*). This is because the surface area of sample 2 is almost three times that of sample 1. The experimentally derived convective thermal resistances are compared to the correlation from Tullius et al. [16] and the average error is 9.05% for sample 1 and 14.33% for sample 2. This correlation will be used again in Sec. 4 to explore the tradeoff between the electrical and thermal performance. As the heat fluxes increase, the fluid temperature increases, which leads to a decrease of pressure drop due to the decrease of viscosity, as shown in Fig. 6(*d*). The average Re in the single-phase region are 171.4 and 25.4 for samples 1 and 2, respectively.

With further increases in heat flux, boiling initiated in the exit manifold outside the finned region, and the flow transitions from single-phase to two-phase. Figure 7 compares results when heat fluxes were high enough to induce boiling in the finned area. Local two-phase heat transfer coefficients are shown in Fig. 7(*a*), and they decrease with increasing heat flux. Similar trends were also reported by Qu and Siu-Ho [12]. Boiling was observed only in the last quarter of the micropin-fin array close to passage exit due to inlet subcooling. Bubble nucleation begins at certain micropin-fins and expands rapidly in a triangular wake of liquid and vapor mixtures, as shown in Fig. 8. The increase of vapor quality in the liquid vapor mixture degraded heat transfer as heat flux increased. A sudden drop in local heat transfer coefficient of sample 2 is observed when the heat flux exceeds 450 W/cm^2. One possible reason is thinning of liquid film and the approach of partial dry out. Figure 7(*b*) shows the boiling curves for both tests, and sample 2 with denser pins had lower wall superheat at the same heat fluxes. When boiling was first observed in the finned area, vapor appeared only at the row of pins closest to the channel exit. As supplied power increased, the vapor front moved toward the channel inlet. At the highest heat fluxes achieved, boiling was observed in the last quarter of the finned area close to the channel exit. Therefore, at the beginning of boiling, the majority of the finned area was still in single-phase, and pressure drop showed

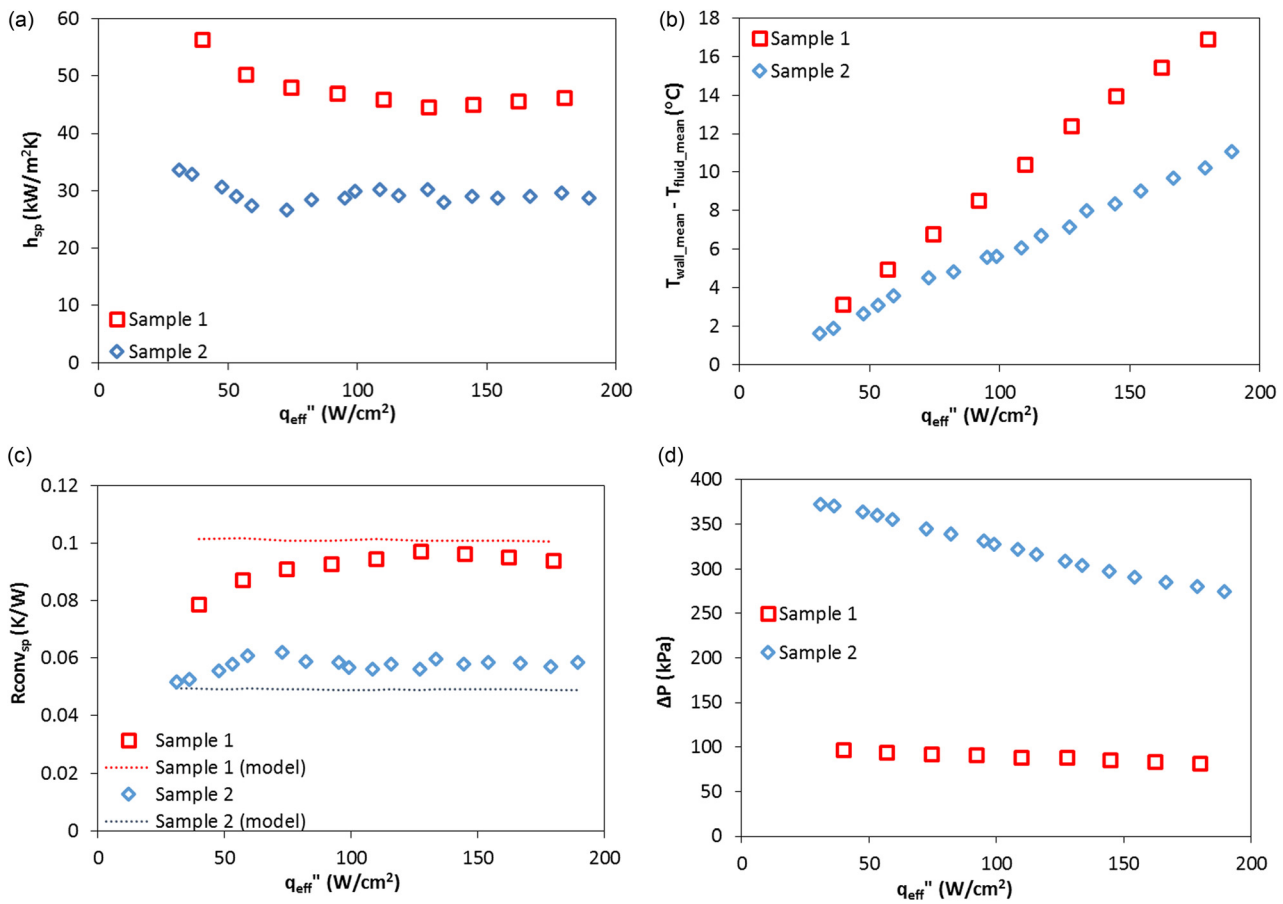

Fig. 6 (*a*) Heat transfer coefficient, (*b*) mean temperature difference from wall to fluid, (*c*) convective resistance, and (*d*) pressure drop for single-phase

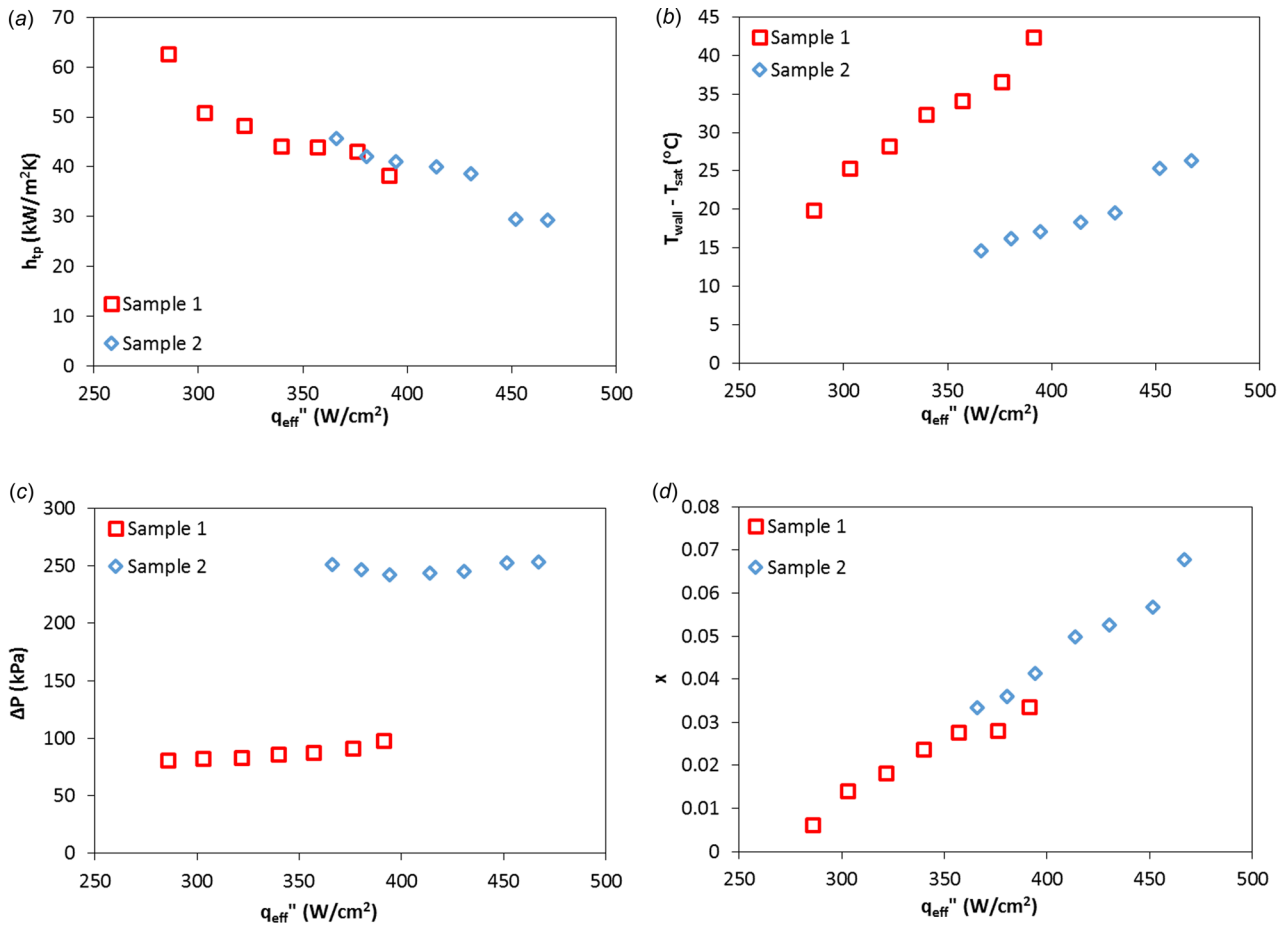

Fig. 7 (*a*) Local two-phase heat transfer coefficient, (*b*) boiling curve, (*c*) pressure drop, and (*d*) vapor quality

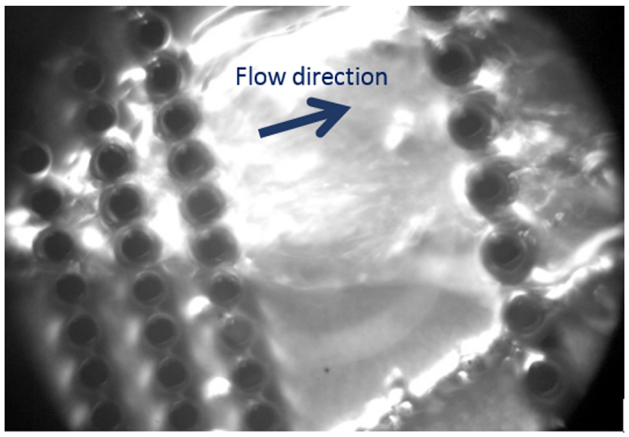

Fig. 8 Flow visualization of sample 1 at 381 W

single-phase (i.e., a decrease with an increase in heat flux) behavior for sample 2 as shown in Fig. 7(*c*). This was not observed for sample 1 because sample 1, with fewer micropin-fins, had lower pressure drop, and the effects of the viscosity decrease due to fluid heating did not overshadow the pressure increase due to existence of vapor phase. Exit vapor qualities are plotted in Fig. 7(*d*), and they increased roughly linearly with increasing heat flux.

By comparing Figs. 6 and 7, it can be found that for the studied micropin-fin dimensions, two-phase cooling can improve the heat transfer coefficient. Increasing the micropin-fin density will increase the pressure drop for the same mass flow rate and can effectively decrease the convective thermal resistance, but not necessarily improve the heat transfer coefficient.

4 Impact of Microfluidic Cooling on Electrical Performance of 3D Interconnects

The impact of the micropin-fin heat sink design on the electrical performance of 3D interconnects is evaluated to be a first-order in this section. Figure 9 shows a simple 3D interconnect link with embedded microfluidic cooling in which a transmitter in tier 1 of the stack communicates with a receiver located in tier 2; the signal transmission occurs through the on-chip wires on tiers 1 and 2 as well as the TSV. The TSVs are embedded within the micropin-fins, which are submerged in coolant.

The 50% delay of the 3D interconnect was evaluated using a simple Elmore model [17] as well as commercial simulation tools to attain an initial insight. The equivalent resistance and capacitance of the driver and receiver were taken from the 2012 ITRS projection for 14 nm CMOS [18]. The wires and TSVs were simulated with ANSYS HFSS software to extract the S-parameters up to 50 GHz [19], which were then imported into AGILENT ADS. The TSV capacitance was extracted from the S-parameters at 2 GHz. For simplicity, the interconnects were ground-signal-ground configured. We assumed the length of the wires on tiers 1 and 2 to be half of the micropin-fin pitch; this was a worst case scenario where the driver and receiver were placed at the center between two micropin-fins. The impact of the coolant was neglected in this analysis.

The 50% delay of the 3D link and wire length versus micropin-fin pitch is shown in Fig. 10(*a*). The micropin-fin height is fixed at 200 μm. As micropin-fin pitch increases, delay increases with pitch because the wire length is assumed to be half of the pitch.

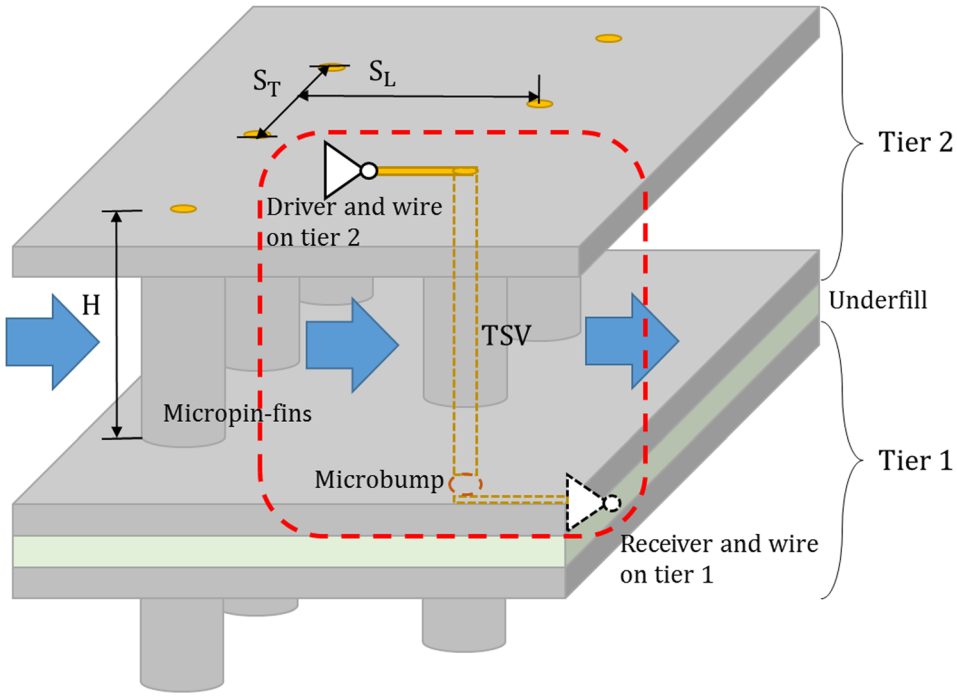

Fig. 9 Three-dimensional interconnect link

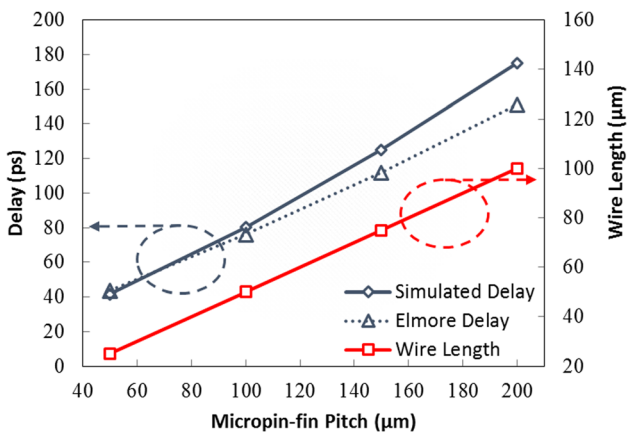

Fig. 10 Delay, wire length, and TSV capacitance versus (*a*) micropin-fin pitch and (*b*) TSV height

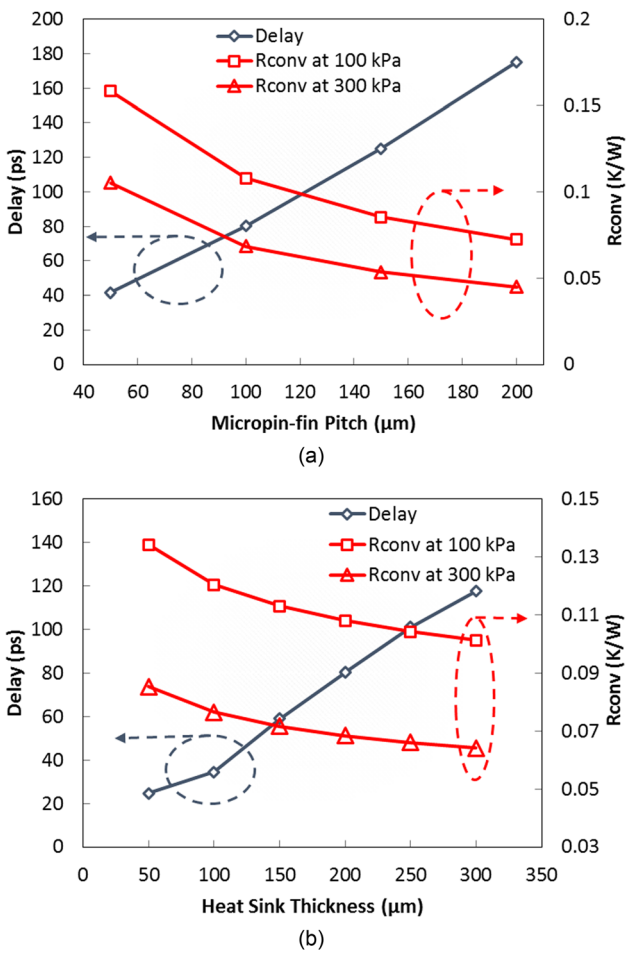

Fig. 11 Delay and R_{CONV} versus (*a*) micropin-fin pitch and (*b*) TSV height

When the micropin-fin pitch is fixed at 100 μm and the micropin-fin height increases, TSV capacitance and link delay increase, as shown in Fig. 10(*b*). While the delay value will change when the impact of the coolant is included, the delay trend versus micropin-fin pitch and heat sink thickness will be similar.

The delay and R_{CONV} versus micropin-fin longitudinal pitch and heat sink thickness are shown in Fig. 11. R_{CONV} is calculated by empirical models [16] for single-phase cooling. In the model, the Nusselt number is calculated by

$$\mathrm{Nu} = 0.08\left(\frac{H_f}{D}\right)^{0.25}\left(\frac{S_L}{D}\right)^{0.2}\left(\frac{S_T}{D}\right)^{0.2}\left(\frac{\mathrm{Pr}}{\mathrm{Pr}_s}\right)^{0.25} \times \left(1+\frac{d_H}{D}\right)^{0.4}\mathrm{Re}^{0.6}\mathrm{Pr}^{0.36} \tag{16}$$

where H_f, D, S_L, and S_T are the micropin-fin height, diameter, longitudinal pitch, and transverse pitch, respectively. We assume that the micropin-fins are bonded to the cap; therefore, the channel clearance d_H is set to be zero.

The average heat transfer coefficient can be calculated as

$$h = \frac{\mathrm{Nu} * k_f}{D} \tag{17}$$

and R_{CONV} is calculated using Eq. (9). In the calculation, pressure drops of 100 kPa and 300 kPa were selected. Increase of either longitudinal pitch or micropin-fin height will lead to an increase of Nusselt number, and therefore, a decrease R_{CONV} in the range of pressure drop and dimensions studied.

A clear tradeoff between the electrical and thermal performance can be observed in Fig. 11(*a*) when the longitudinal pitch increases, R_{CONV} decreases. However, the link delay increases due to longer wires connecting the TSVs embedded in the micropin-fins. In Fig. 11(*b*), increasing micropin-fin height can decrease R_{CONV}, but it will increase TSV height and capacitance and therefore increase the delay.

5 Conclusion

In this work, staggered micropin-fin heat sinks were designed, fabricated, and tested. The measured maximum heat transfer coefficient reached up to 60 kW/m^2 K for the sample with lower micropin-fin density and 45 kW/m^2 K for the sample with higher micropin-fin density. Even though increasing micropin-fin density does not necessarily increase the heat transfer coefficient, the heat sink with higher micropin-fin density has lower thermal resistance under the same mass flow rate, due to an increase in the total heat transfer area. In the single-phase region, the convective thermal resistance was compared with an empirical model. The impact of microfluidic cooling on the electrical performance, e.g., electric signal delay, of 3D interconnect links was explored with respect to various dimensions of the heat sink. It has been shown that a tradeoff exists between improving the heat transfer performance but increasing capacitive latency of the 3D interconnect links.

Acknowledgment

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Nomenclature

A_c = single micropin-fin cross section area
$A_{c,\min}$ = minimum heat sink cavity cross section area
A_f = single micropin-fin surface area
A_h = total heated area
A_t = total area exposed to fluid
A_{uc} = unit cell area of single micropin-fin
C_p = specific heat capacity
D = pin diameter
d_H = channel clearance
h = average heat transfer coefficient
H_f = micropin-fin height
h_{sp} = single-phase heat transfer coefficient
h_{tp} = two-phase heat transfer coefficient
k_f = thermal conductivity of fluid
k_s = thermal conductivity of solid
k_{Si} = thermal conductivity of silicon
k_{SiO_2} = thermal conductivity of silicon dioxide
m = micropin-fin efficiency parameter
$\dot{m}$ = mass flow rate of water
N_t = total number of micropin-fins
Nu = Nusselt number
P_f = micropin-fin perimeter
P_{total} = total power supplied to device
Pr = Prandtl number
Q_{loss} = heat loss
q''_{eff} = effective heat flux
R_{CONV} = convective thermal resistance
Re = Reynolds number
S_L = longitudinal pitch
S_T = transverse pitch
T_h = heater temperature
T_w = wall temperature
t_{Si} = heat sink base silicon thickness
t_{SiO_2} = thickness of silicon dioxide
T_{sat} = saturation temperature
$\bar{T}_{m,f}$ = mean fluid temperature
$\bar{T}_{m,w}$ = mean wall temperature
W_{ch} = heat sink cavity width
η_f = fin efficiency
η_o = overall fin efficiency

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